DVCon U.S. 2022 Announces Call for Panel, Short Workshop and Tutorial Proposals

Deadline for submissions is September 14


Panels
DVCon U.S. will host two panel discussions. The one-hour panels should be lively, can be controversial, and should provoke engaging discussion on a topic of interest to the community.

Suggested topics include: Experiences using design and/or verification IP for SoC development; Experiences applying machine-learning techniques; Efficient adoption of Cloud resources; Efficient deployment of compute, networking, and storage resources; Experiences adopting functional-safety related standards such as ISO26262, DO-254, etc.; Design and verification sign-off and closure; Dealing with the technical and logistical challenges of multi-site projects; Developing, adopting and proliferating new standards; Experiences deploying a verification methodology library, especially the deployment of UVM; Designing and/or verifying complex ASICs and FPGAs using multiple HDLs and/or HVLs in a design cycle; Recovering from Covid-19 pandemic and lessons learned to cope with future disruptions

More information and guidelines can be found here.

Sponsored Short Workshops
Short workshops are sponsored 90-minute sessions. DVCon offers short workshops to provide more opportunities for participation from companies and exhibitors, especially smaller organizations, at an affordable level.

Sponsored Tutorials
The three-hour DVCon U.S. tutorials are available to all attendees and are included in full conference registration. The Committee is seeking sponsored tutorial topics that are current, have a high-level of interest and offer strong continuing educational content.
Suggested Topics
Suggested topics for both workshops and tutorials include: Application-specific design verification challenges, techniques; Assertion-based Verification, SystemVerilog Assertions, PSL, etc.; Coverage-driven Verification; Debug for design and verification; Embedded software verification; Emulation; Formal Methodology and Static Analysis; FPGA Prototyping; Functional Safety and Security; Hardware/Software Co-development; High-level Synthesis; Low-power Design and Verification techniques; Machine Learning applications for verification and design; Mixed-signal modeling and verification; Moving from proprietary solutions to standards-based design and verification; Open source hardware/software/architecture.; Portable Stimulus; Post SI Debug; Secure/Encrypted IP-based SoC design methods; SoC and Software-driven Verification; SystemC /C/C++ Design and/or Verification of systems; SystemVerilog for Verification and/or Design; Transaction Level Modeling (TLM), ESL Design, and IP integration (IP-XACT); Verification Productivity Methods;

Proposals
Proposals should be an abstract of the workshop or tutorial, two to five paragraphs and no more than 1,000 words.

Additional Information and Pricing
For more information on workshops, including pricing, visit here.
For more information on tutorials, including pricing, visit here.

Submission Deadline for Panel, Workshop and Tutorial Proposals
The deadline to submit panel, workshop and tutorial proposals is September 14, 2021.

About DVCon
DVCon is the premier conference for discussion of the functional design and verification of electronic systems. DVCon is sponsored by Accellera Systems Initiative, an independent, not-for-profit organization dedicated to creating design and verification standards required by systems, semiconductor, intellectual property (IP) and electronic design automation (EDA) companies. For more information about Accellera, please visit www.accellera.org. For more information about DVCon U.S., please visit here. Follow DVCon on Facebook, LinkedIn or @dvcon_us on Twitter or to comment, please use #dvcon_us.

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